Integrated Circuit Systems, Inc.

ICS8427-02

500MHz, Low Jitter LVCMOS/Crystal-to-LVHSTL Frequency Synthesizer

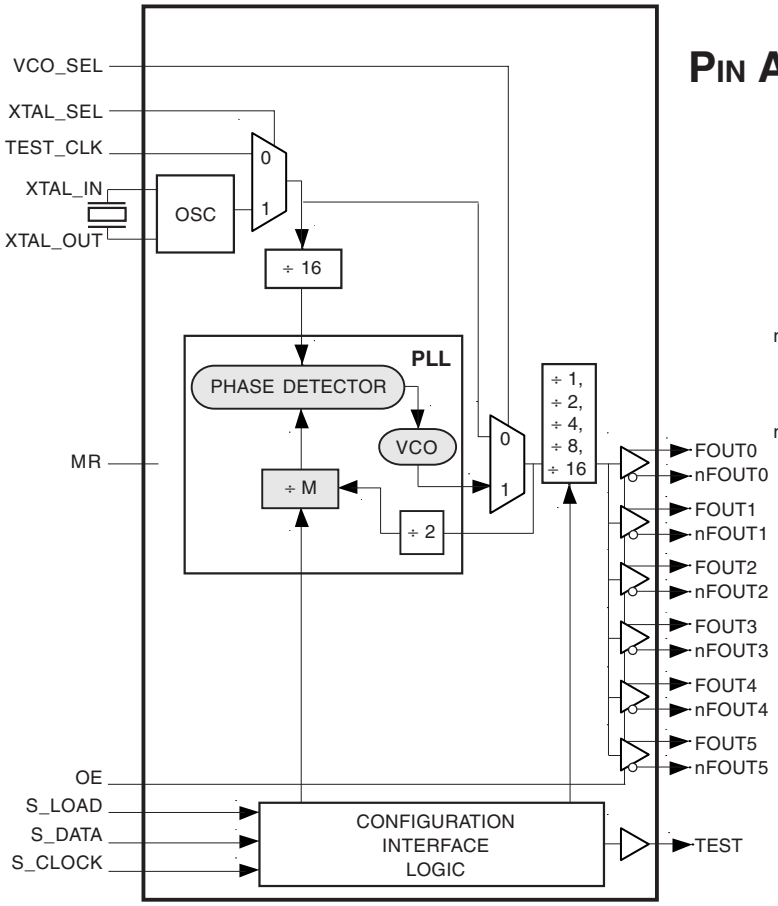
General Description

The ICS8427-02 is a general purpose, six LVHSTL output high frequency synthesizer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8427-02 can support a very wide output frequency range of 15.625MHz to 500MHz. The device powers up at a default output frequency of 200MHz with a 16.6667MHz crystal interface, and the frequency can then be changed using the serial programming interface to change the M feedback divider and N output divider. Frequency steps as small as 125kHz can be achieved using a 16.6667MHz crystal and the output divider set for ÷16. The low jitter and frequency range of the ICS8427-02 make it an ideal clock generator for most clock tree applications.

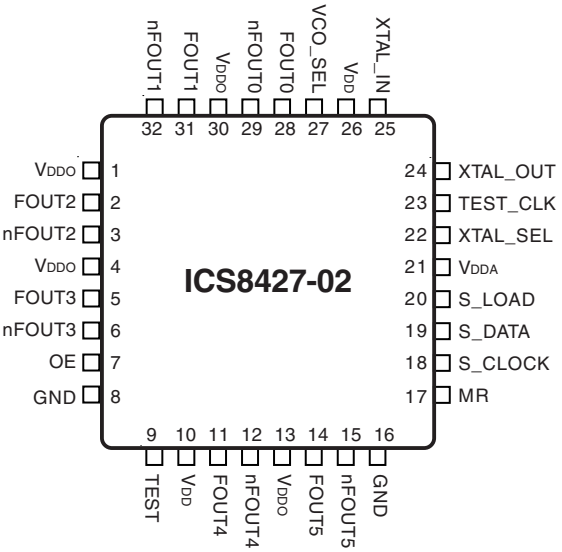
Features

- Six differential LVHSTL outputs
- Selectable crystal input interface or TEST_CLK input
- TEST_CLK accepts the following input types: LVCMOS, LVTTL
- Output frequency range: 15.625MHz to 500MHz
- VCO range: 250MHz to 500MHz
- Serial interface for programming feedback and output dividers
- Supports SSC, -0.5% downspread. Can be enabled through use of the serial programming interface.
- Output skew: 100ps (maximum)
- Cycle-to-cycle jitter: 50ps (maximum)
- 2.5V core/1.8V output supply voltage
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in both standard and lead-free RoHS-compliant packages

Block Diagram



Pin Assignment



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

32-Lead VFQFN
5mm x 5mm x 0.75mm package body
K Package
Top View

Functional Description

NOTE: The functional description that follows describes operation using a 16.6667MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 6 NOTE 1.

The ICS8427-02 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A parallel-resonant, fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is divided by 16 prior to the phase detector. With a 16.6667MHz crystal, this provides a 1.0417MHz reference frequency. The VCO of the PLL operates over a range of 250MHz to 500MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be 2M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The ICS8427-02 powers up by default to 200MHz output frequency, using a 16.6667MHz crystal (M = 192, N = 2). The output frequency can be changed after power-up by using the serial interface to program the M feedback divider and the N output divider.

The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows:

$$fVCO = \frac{fxtal}{16} \times 2M$$

The M value and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function Table. Valid M values for which the PLL will achieve lock for a 16.6667MHz reference are defined as $120 \leq M \leq 240$. The frequency out is defined as follows: $fout = \frac{fVCO}{N} = \frac{fxtal}{16} \times \frac{2M}{N}$

Serial operation occurs when S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider and N output divider when S_LOAD transitions from LOW-to-HIGH. The M divide and N output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider and N outputdivider on each rising edge of S_CLOCK. The serial mode can be used to program the M and N bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

T1	T0	TEST Output
0	0	LOW
0	1 (Power-up Default)	S_Data, Shift Register Input
1	0	Output of M divider
1	1	CMOS Fout

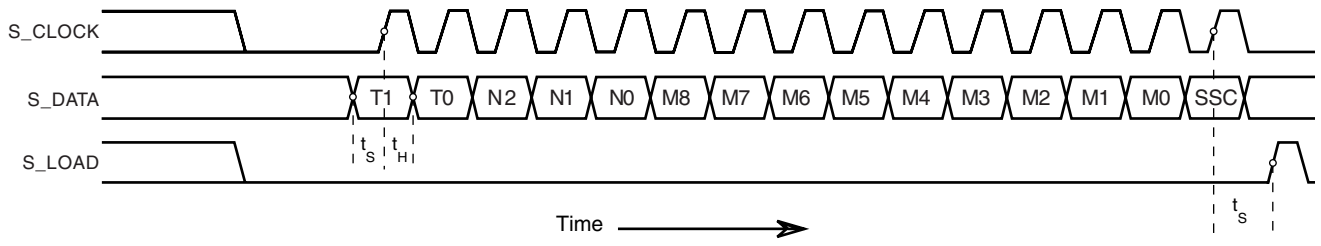
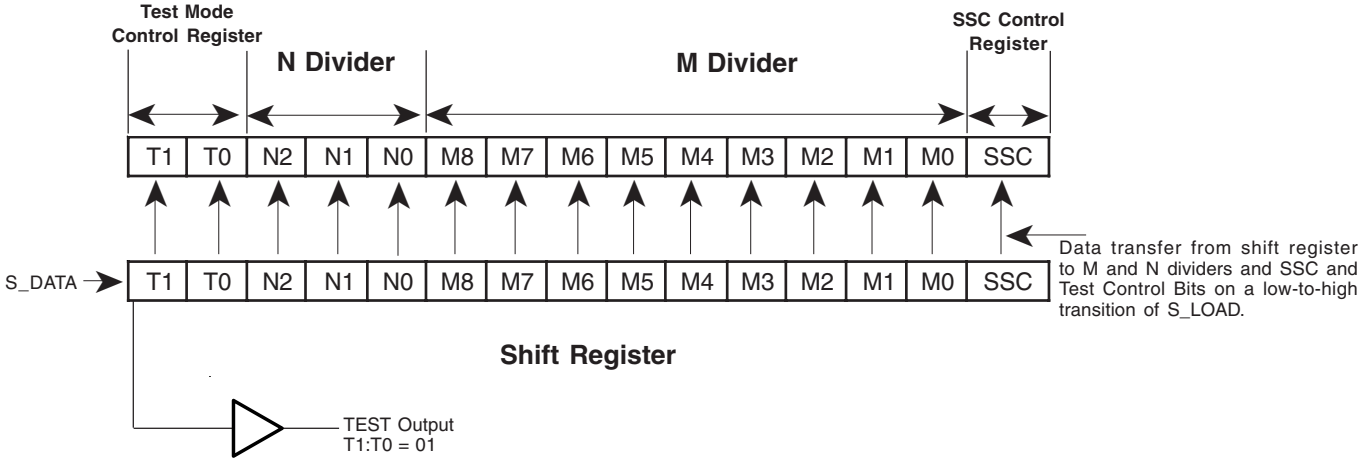


Figure 1. Serial Load Operations

NOTE: Default Output Frequency, using a 16.6667MHz crystal on power-up = 200MHz (M = 192, N = 2) SSC off

M and N Dividers, SSC and Test Mode Control Bits



ICS8427-02 Shift Register Operation – Read Back Capability

1. Device powers up by default in Test Mode 01.
   The Test Output in this case is wired to the shift register.

2. Shift in serial data stream and latch into M, N, T1, T0 and SSC Control Bits.
   Shift in T1:T0=00, so that the TEST Output will be turned off after the bits are shifted in and latched.

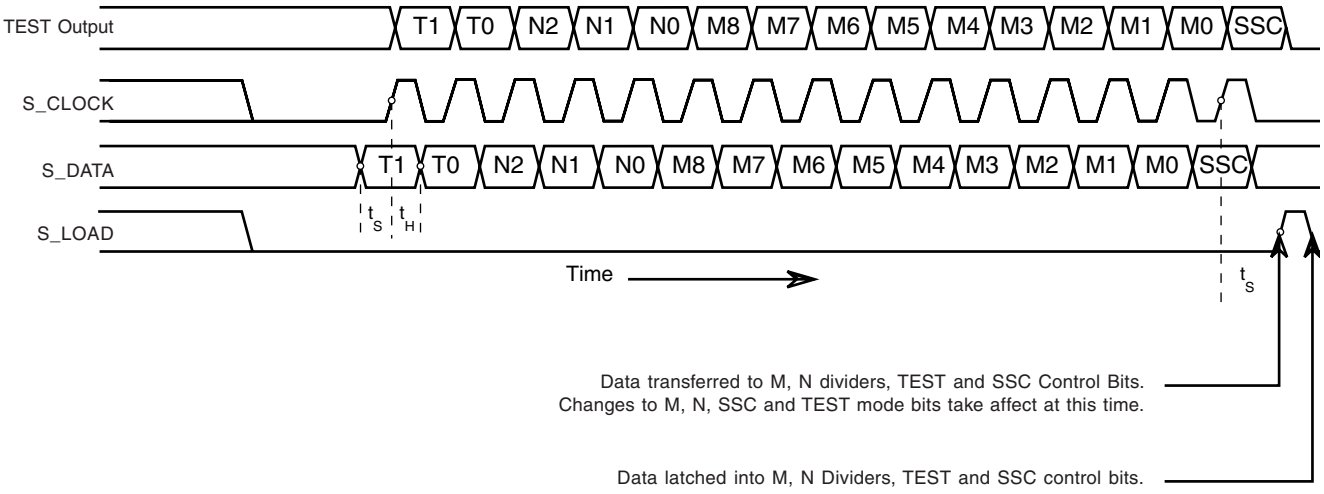


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 4, 13, 30	V_{DDO}	Power		Output supply pins.
2, 3	FOUT2, nFOUT2	Output		Differential output pair. HSTL interface levels.
5, 6	FOUT3, nFOUT3	Output		Differential output pair. HSTL interface levels.
7	OE	Input	Pullup	Active High output enable. When HIGH, the outputs are enabled. When LOW, FOUTx = Low, nFOUTx = High. LVCMOS/LVTTL interface levels.
8, 16	GND	Power		Power supply ground.
9	TEST	Output		Test output which is ACTIVE in the serial mode of operation. LVCMOS/LVTTL interface levels.
10, 26	V_{DD}	Power		Core supply pins.
11, 12	FOUT4, nFOUT4	Output		Differential output pair. HSTL interface levels.
14, 15	FOUT5, nFOUT5	Output		Differential output pair. HSTL interface levels.
17	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs FOUTx to go low and the inverted outputs nFOUTx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
18	S_CLOCK	Input	Pullup	Input clock to load serial S_DATA into the shift register. LVCMOS/LVTTL interface levels.
19	S_DATA	Input	Pullup	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.
20	S_LOAD	Input	Pulldown	Controls transition of data from shift register into the dividers. LVCMOS/LVTTL interface levels.
21	V_{DDA}	Power		Analog supply pin.
22	XTAL_SEL	Input	Pullup	Selects between XTAL input or test input as the PLL reference source. Selects XTAL input when HIGH. Selects TEST_CLK when LOW. LVCMOS/LVTTL interface levels.
23	TEST_CLK	Input	Pulldown	Test clock input. LVCMOS/LVTTL interface levels.
24, 25	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
27	VCO_SEL	Input	Pullup	Determines whether synthesizer is in PLL or bypass mode. LVCMOS/LVTTL interface levels.
28, 29	FOUT0, nFOUT0	Output		Differential output pair. HSTL interface levels.
31, 32	FOUT1, nFOUT1	Output		Differential output pair. HSTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Table 3A. Control Input Function Table

Inputs			Outputs	
OE	**XTAL_SEL**	**Selected Source**	**FOUT0:FOUT5**	**nFOUT0:nFOUT5**
0	0	TEST_CLK	Disabled; LOW	Disabled; HIGH
0	1	XTAL_IN, XTAL_OUT	Disabled; LOW	Disabled; HIGH
1	0	TEST_CLK	Enabled	Enabled
1	1	XTAL_IN, XTAL_OUT	Enabled	Enabled

After OE switches, the clock outputs are disabled or enabled following a rising and falling VCO edge as shown in *Figure 2.*

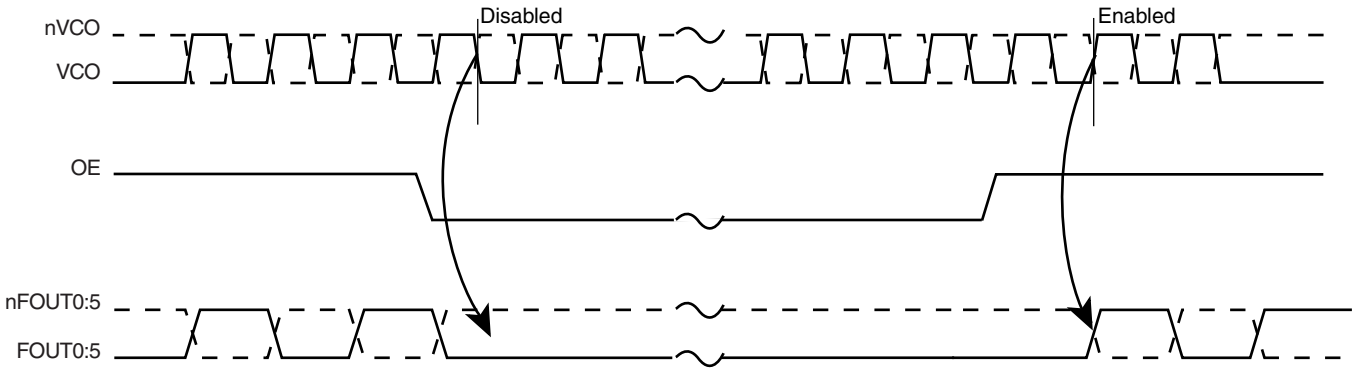


Figure 2. OE Timing Diagram

Table 3B. Programmable VCO Frequency Function Table[NOTE 1]

VCO Frequency (MHz)	M Divide	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
250	120	0	0	1	1	1	1	0	0	0
252.08	121	0	0	1	1	1	1	0	0	1
254.17	122	0	0	1	1	1	1	0	1	0
•	•	•	•	•	•	•	•	•	•	•
400	192	0	1	1	0	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•	•
497.92	239	0	1	1	1	0	1	1	1	1
500	240	0	1	1	1	1	0	0	0	0

NOTE 1: These M divide values and the resulting frequencies correspond to an input frequency of 16.6667MHz.

Table 3C. Serial Mode Function Table

Inputs				Conditions
MR	S_LOAD	S_CLOCK	S_DATA	
H	X	X	X	Reset. Forces outputs differential LOW. FOUTx = Low, nFOUTx = High.
L	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
L	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
L	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
L	↓	L	Data	M divider and N output divider values are latched.
L	L	X	X	Serial input do not affect shift registers.
L	H	↑	Data	S_DATA passed directly to M divider as it is clocked.

NOTE: L = LOW
H = HIGH
X = Don't care
↑ = Rising edge transition
↓ = Falling edge transition

Table 3D. Programmable Output Divider Function Table

Input			N Divider Value	Output Frequency (MHz)	
N2	N1	N0		Minimum	Maximum
0	0	0	2	125	250
0	0	1	4	62.5	125
0	1	0	8	31.25	62.5
0	1	1	16	15.625	31.25
1	0	0	1	250	500
1	0	1	2	125	250
1	1	0	4	62.5	125
1	1	1	8	31.25	62.5

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	
for 32 Lead LQFP	47.9°C/W (0 lfpm)
for 32 Lead VFQFN	34.8°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply		2.375	2.5	2.625	V
V_{DDA}	Analog Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current				175	mA
I_{DDA}	Analog Supply Current				15	mA
I_{DD0}	Output Supply Current	No Load		0		mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDA} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.7	V
I_{IH}	Input High Current	MR, S_LOAD, TEST_CLK	$V_{DD} = V_{IN} = 2.625V$			150	µA
		XTAL_SEL, VCO_SEL, S_CLOCK, S_DATA, OE	$V_{DD} = V_{IN} = 2.625V$			5	µA
I_{IL}	Input Low Current	MR, S_LOAD, TEST_CLK	$V_{DD} = 2.625V$, $V_{IN} = 0V$	-5			µA
		XTAL_SEL, VCO_SEL, S_CLOCK, S_DATA, OE	$V_{DD} = 2.625V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage	TEST; NOTE 1		1.5			V
V_{OL}	Output Low Voltage	TEST; NOTE 1				0.4	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$.

Table 4C. LVHSTL DC Characteristics, $V_{DD} = V_{DDA} = 2.5V±5\%$, $V_{DDO} = 1.8V±0.2V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		0.9		1.3	V
V_{OL}	Output Low Voltage; NOTE 1		0		0.4	V
V_{OX}	Output Crossover Voltage; NOTE 2		40		60	%
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.1	V

NOTE 1: Outputs terminated with 50Ω to GND. See 2.5V *Output Load Test Circuit figure* in the Parameter Measurement Information section.
NOTE 2: Defined with respect to output voltage swing at a given condition.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		12		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

Table 6. Input Characteristics, $V_{DD} = V_{DDA} = 2.5V±5\%$, $V_{DDO} = 1.8V±0.2V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	TEST_CLK	VCO select = 1	12		40	MHz
			VCO select = 0 (bypass mode)			400	MHz
		XTAL; NOTE 1		12		40	MHz
		S_CLOCK				50	MHz
t_{r_INPUT}	Input Rise Time	TEST_CLK				5	ns

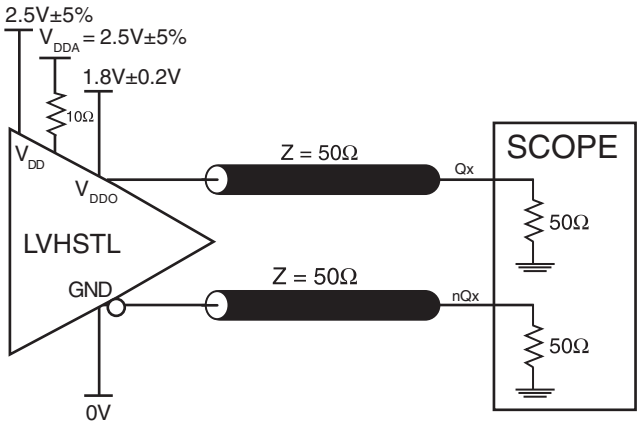
NOTE 1: For the crystal frequency range the M value must be set to achieve the minimum or maximum VCO frequency range of 250MHz or 500MHz. Using the minimum frequency of 12MHz valid values of M are $167 \le M \le 256$. Using the maximum frequency of 40MHz valid values of M are $50 \le M \le 100$.

Table 7. AC Characteristics, $V_{DD} = V_{DDA} = 2.5V±5\%$, $V_{DDO} = 1.8V±0.2V$, $T_A = 0°C$ to $70°C$

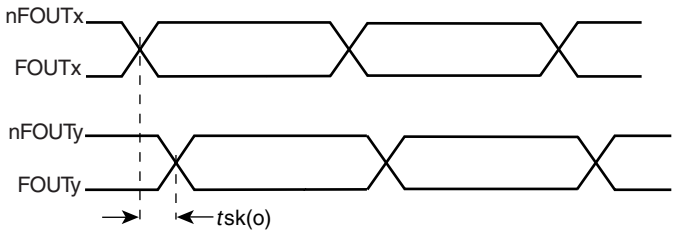
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
F_{MAX}	Output Frequency					500	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1, 3		F_{OUT} = 200MHz		30	50	ps
			F_{OUT} = 267MHz		30	50	ps
			F_{OUT} = 333MHz		30	50	ps
			F_{OUT} = 400MHz		30	50	ps
*t*jitt(T50)	T50 Cycle Jitter		F_{OUT} = 200MHz			200	ps
			F_{OUT} = 267MHz			200	ps
			F_{OUT} = 333MHz			200	ps
			F_{OUT} = 400MHz			200	ps
*t*jit(per)	Period Jitter, RMS; NOTE 1				2.5	5	ps
*t*sk(o)	Output Skew; NOTE 2, 3				65	100	ps
F_M	SSC Modulation Frequency; NOTE 4, 5		F_{OUT} = 200MHz	30		33.33	kHz
			F_{OUT} = 267MHz	30		33.33	kHz
			F_{OUT} = 333MHz	30		33.33	kHz
			F_{OUT} = 400MHz	30		33.33	kHz
F_{MF}	SSC Modulation Factor; NOTE 4, 5		F_{OUT} = 200MHz		0.3	0.6	%
			F_{OUT} = 267MHz		0.4	0.6	%
			F_{OUT} = 333MHz		0.3	0.6	%
			F_{OUT} = 400MHz		0.3	0.6	%
SSC_{red}	Spectral Reduction; NOTE 4, 5		F_{OUT} = 200MHz	-7	-10		dB
			F_{OUT} = 267MHz	-7	-12		dB
			F_{OUT} = 333MHz	-7	-11		dB
			F_{OUT} = 400MHz	-7	-12		dB
Ref_{spur}	Reference Spur		F_{OUT} = 200MHz		-40		dB
			F_{OUT} = 267MHz		-40		dB
			F_{OUT} = 333MHz		-45		dB
			F_{OUT} = 400MHz		-50		dB
t_R / t_F	Output Rise/Fall Time		20% to 80%	333		667	ps
t_S	Setup Time	S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
t_H	Hold Time	S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
odc	Output Duty Cycle		N = 1	40		60	%
			N = 2	45		55	%
t_{LOCK}	PLL Lock Time					1	ms

See Parameter Measurement Information section.
NOTE 1: Jitter performance using XTAL inputs.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Spread Spectrum clocking enabled.
NOTE 5: Using a 16.6667MHz quartz crystal.

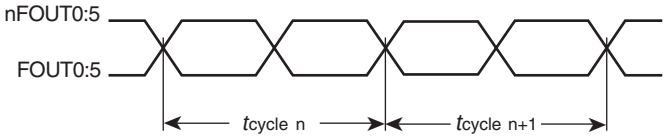
Parameter Measurement Information



2.5V Core/1.8V Output Load AC Test Circuit

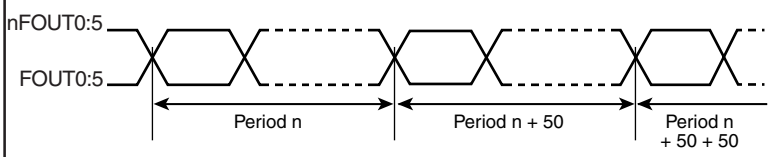


Output Skew



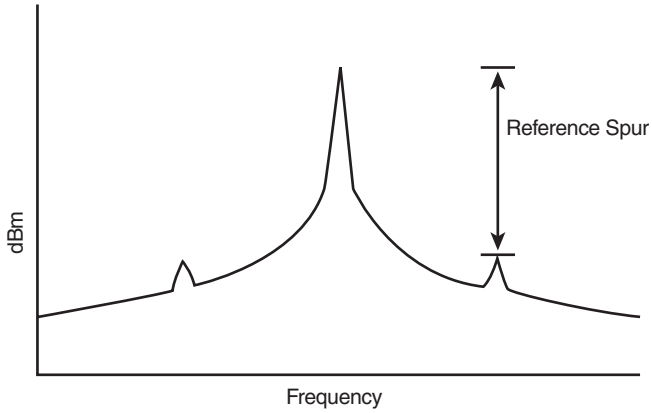
$t$jit(cc) = $t$cycle n – $t$cycle n+1
1000 Cycles

Cycle-to-Cycle Jitter

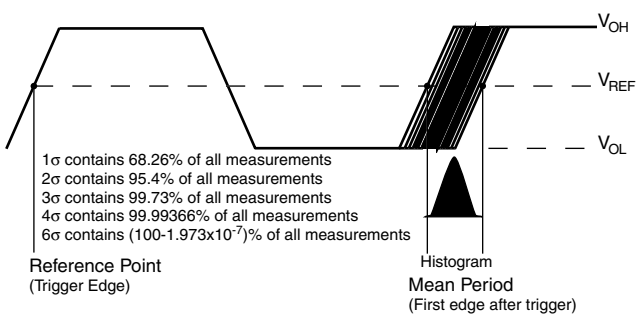


$t$jit (50) = Period n – Period n +50
Minimum 16,667 consective cycles
334 measurements

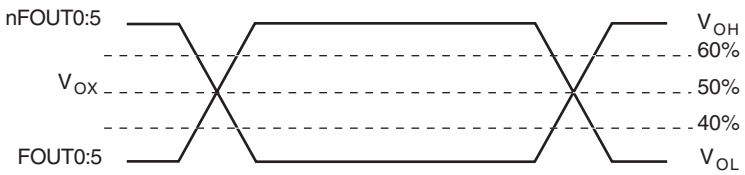
T50 Cycle-to-Cycle Jitter



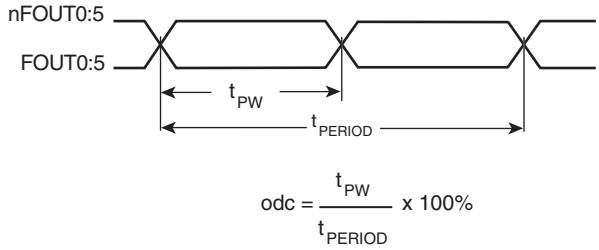
Spur Reduction



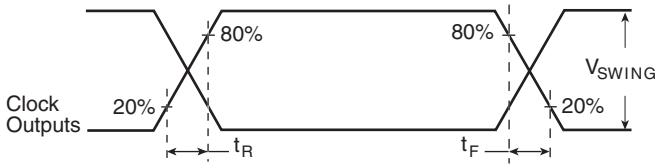
Period Jitter



Output Crossover Voltage



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Input:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

TEST_CLK Input:
For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the TEST_CLK to ground.

LVCMOS Control Pins:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVHSTL Output
All unused LVHSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The ICS8427-02 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 3* below were determined using a 16.66MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

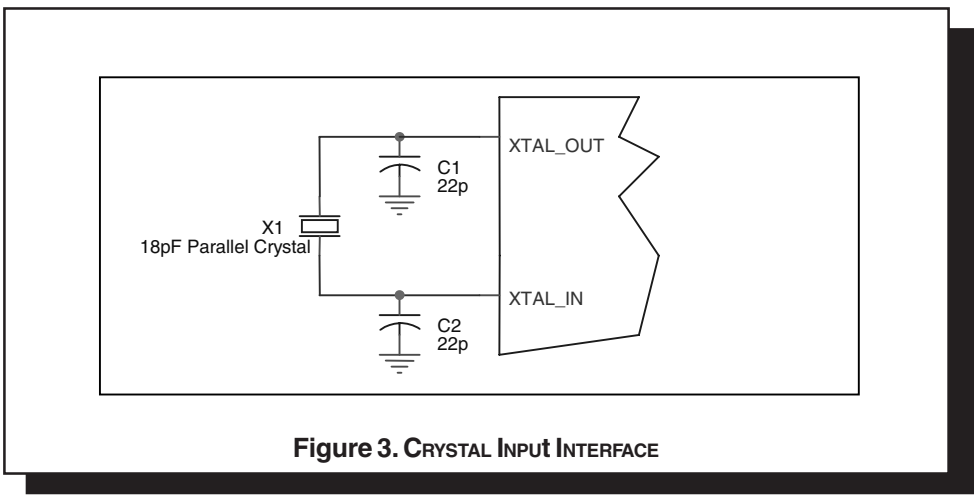


Figure 3. Crystal Input Interface

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8427-02 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 4* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

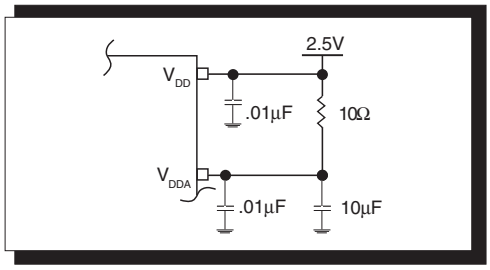


Figure 4. Power Supply Filtering

Spread Spectrum

Spread-spectrum clocking is a frequency modulation technique for EMI reduction. When spread-spectrum is enabled, a 32.55kHz triangle waveform is used with 0.5% down-spread (+0.0%/-0.5%) from the nominal 200MHz clock frequency. An example of a triangle frequency modulation profile is shown in *Figure 5A* below. The ramp profile can be expressed as:

- Fnom = Nominal Clock Frequency in Spread OFF mode (200MHz with 16.6667MHz IN)
- Fm = Nominal Modulation Frequency
  $= \frac{\text{Reference Frequency}}{16 \times 32}$
- δ = Modulation Factor (0.5% down spread)

$(1 - \delta)\ fnom + 2\ fm \times \delta \times fnom \times t$ when $0 < t < \frac{1}{2\ fm}$,

$(1 - \delta)\ fnom - 2\ fm \times \delta \times fnom \times t$ when $\frac{1}{2\ fm} < t < \frac{1}{fm}$

The ICS8427-02 triangle modulation frequency deviation will not exceed 0.6% down-spread from the nominal clock frequency (+0.0%/-0.5%). An example of the amount of down spread relative to the nominal clock frequency can be seen in the frequency domain, as shown in *Figure 5B.* The ratio of this width to the fundamental frequency is typically 0.4%, and will not exceed 0.6%. The resulting spectral reduction will be greater than 7dB, as shown in Figure 5B. It is important to note the ICS8427-02 7dB minimum spectral reduction is the component-specific EMI reduction, and will not necessarily be the same as the system EMI reduction.

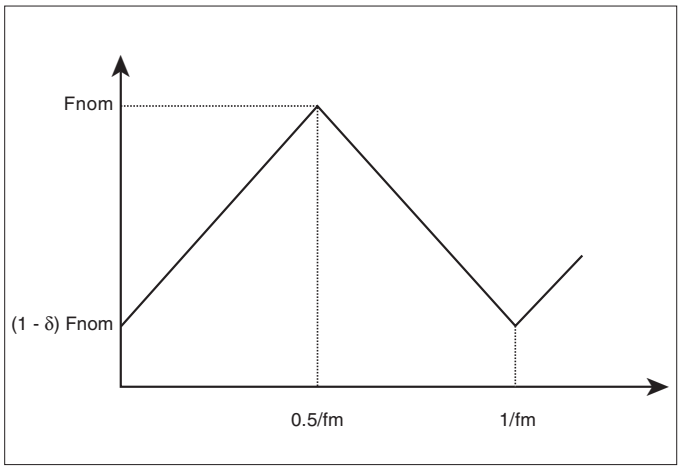


Figure 5A. Triangle Frequency Modulation

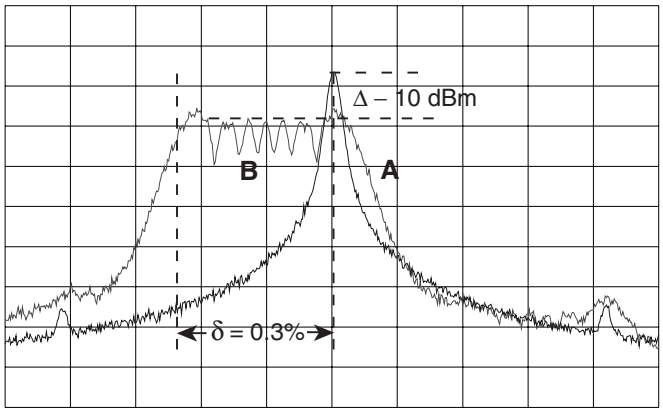


Figure 5B. 200MHz Clock Output in Frequency Domain

(A) Spread-Spectrum OFF
(B) Spread-Spectrum ON

Layout Guideline

Figure 6 shows an application schematic example of the ICS8427-02. In this example, a 16.6667MHz, 18 pF parallel resonant crystal is used. The C1=22pF and C2=22pF are approximate values for frequency accuracy. The C1 and C2 may be slightly adjusted for optimizing frequency accuracy.

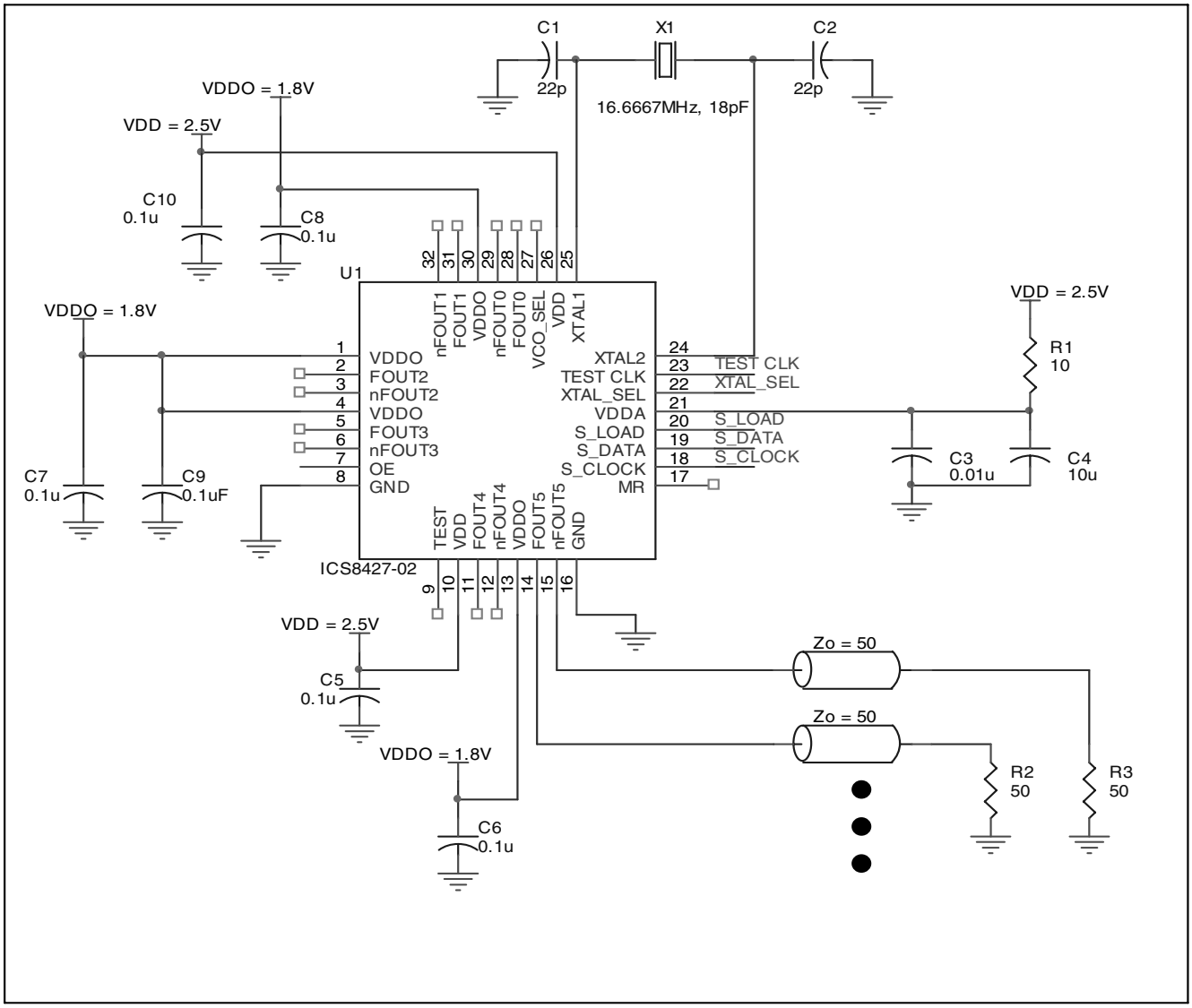


Figure 6. Schematic of Recommended Layout

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8427-02.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS8427-02 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 2.625V * 175mA = **459.4mW**
- Power $(outputs)_{MAX}$ = **32.6mW/Loaded Output pair**
  If all outputs are loaded, the total power is 6 * 32.6mW = **195.6mW**

Total Power $_{MAX}$ (3.465V, with all outputs switching) = 459.37mW + 195.6mW = **655mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 8A below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.655W * 42.1°C/W = 97.6°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 8A. Thermal Resistance θ_{JA} for 32-Pin LQFP, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Table 8B. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

θ_{JA} by Velocity (Linear Feet per Minute)	0
Multi-Layer PCB, JEDEC Standard Test Boards	34.8°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVHSTL output driver circuit and termination are shown in *Figure 7.*

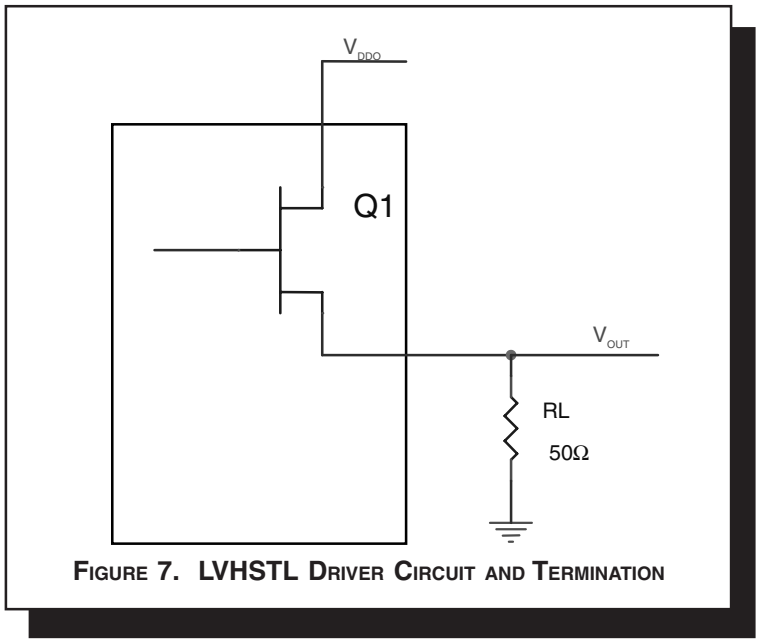


Figure 7. LVHSTL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = (V_{OH\_MIN}/R_L) * (V_{DD\_MAX} - V_{OH\_MIN})$

$Pd\_L = (V_{OL\_MAX}/R_L) * (V_{DD\_MAX} - V_{OL\_MAX})$

Pd_H = (0.9V/50Ω) * (2V - 0.9V) = **19.8mW**
Pd_L = (0.4V/50Ω) * (2V - 0.4V) = **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32.6mW**

Reliability Information

Table 9A. θ_{JA} vs. Air Flow Table for 32 Lead LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Table 9B. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

θ_{JA} 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	34.8°C/W

Transistor Count

The transistor count for ICS8427-02 is: 4585

Package Outline - Y Suffix for 32 Lead LQFP

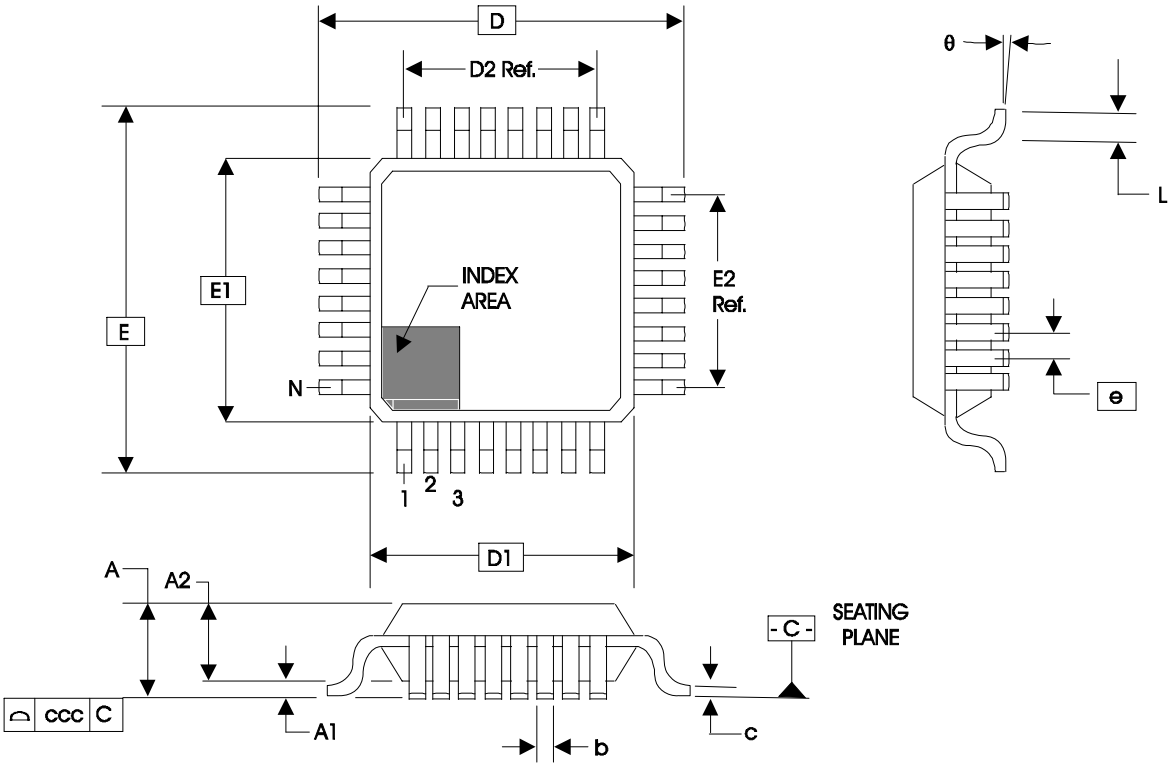


Table 10A. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60	
e		0.80 BASIC	
L	0.45	0.60	0.75
q	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

Package Outline - K Suffix for a 32 Lead VFQFN

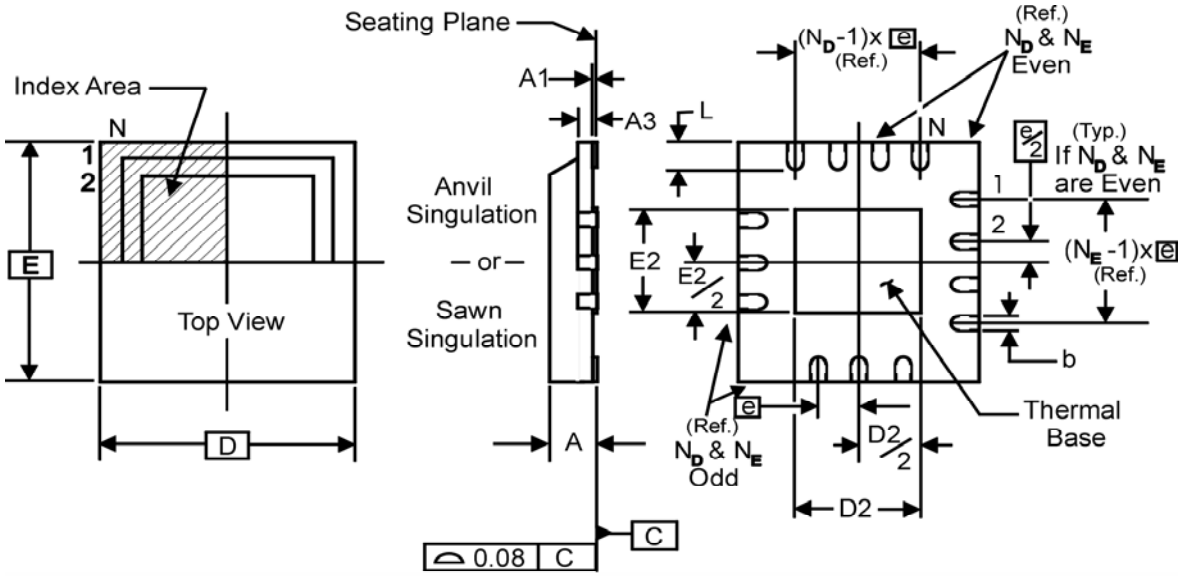


Table 10B. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	VHHD-2		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	0.80	--	1.00
A1	0	--	0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D			8
N_E			8
D		5.00 BASIC	
D2	1.25	2.25	3.25
E		5.00 BASIC	
E2	1.25	2.25	3.25
e		0.50 BASIC	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8427DY-02	ICS8427DY-02	32 Lead LQFP	tray	0°C to 70°C
ICS8427DY-02T	ICS8427DY-02	32 Lead LQFP	1000 tape & reel	0°C to 70°C
ICS8427DY-02LF	ICS8427DY02L	32 Lead "Lead-Free" LQFP	tray	0°C to 70°C
ICS8427DY-02LFT	ICS8427DY02L	32 Lead "Lead-Free" LQFP	1000 tape & reel	0°C to 70°C
ICS8427DK-02	ICS8427DK-02	32 Lead VFQFN	tray	0°C to 70°C
ICS8427DK-02T	ICS8427DK-02	32 Lead VFQFN	2500 tape & reel	0°C to 70°C
ICS8427DK-02LF	TBD	32 Lead "Lead-Free" VFQFN	tray	0°C to 70°C
ICS8427DK-02LFT	TBD	32 Lead "Lead-Free" VFQFN	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T11	10 20	Updated Output Load AC Test Circuit diagram. Ordering Information Table - added lead-free marking for LQFP package.	2/17/06